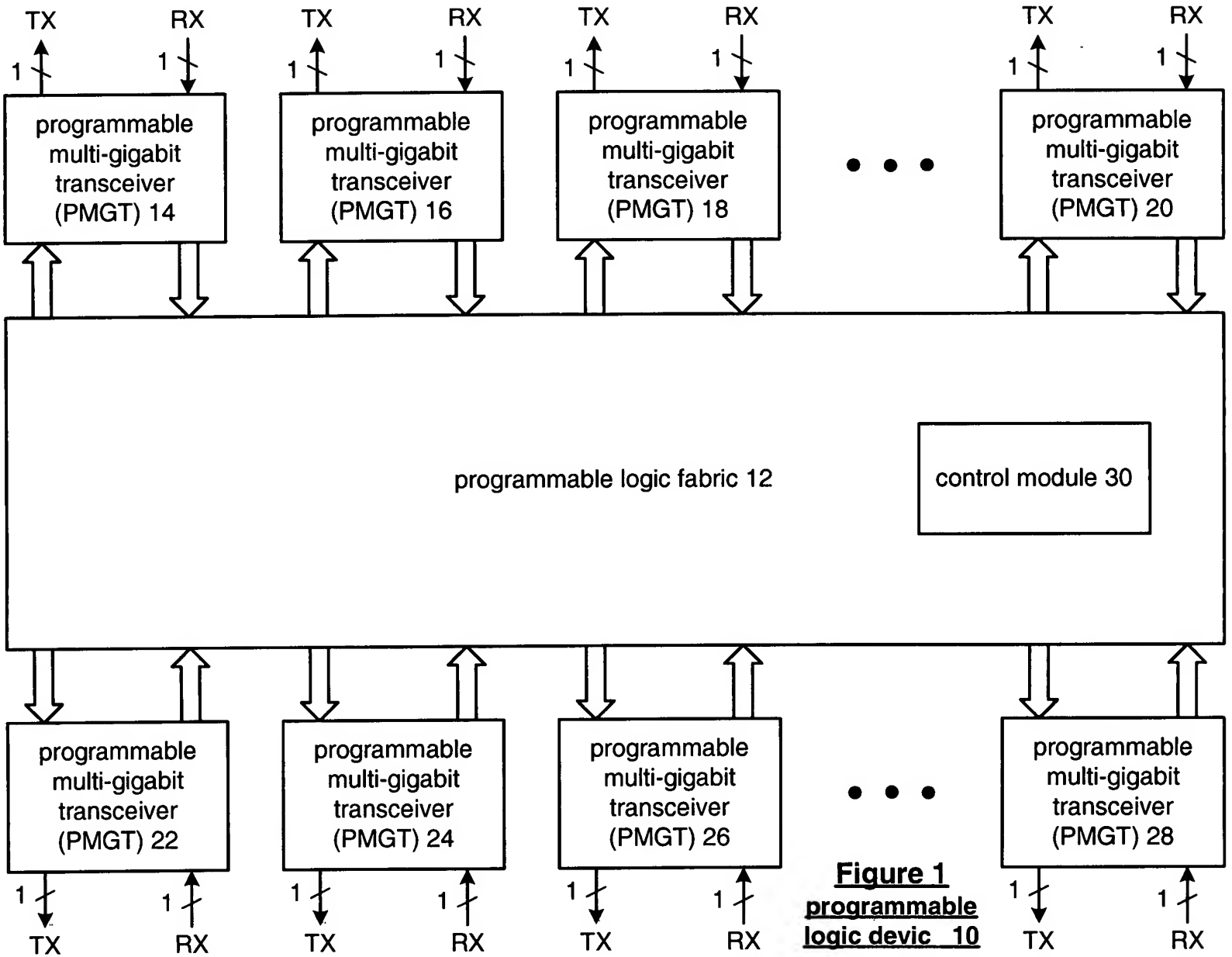


Figure 1
programmable logic devic 10

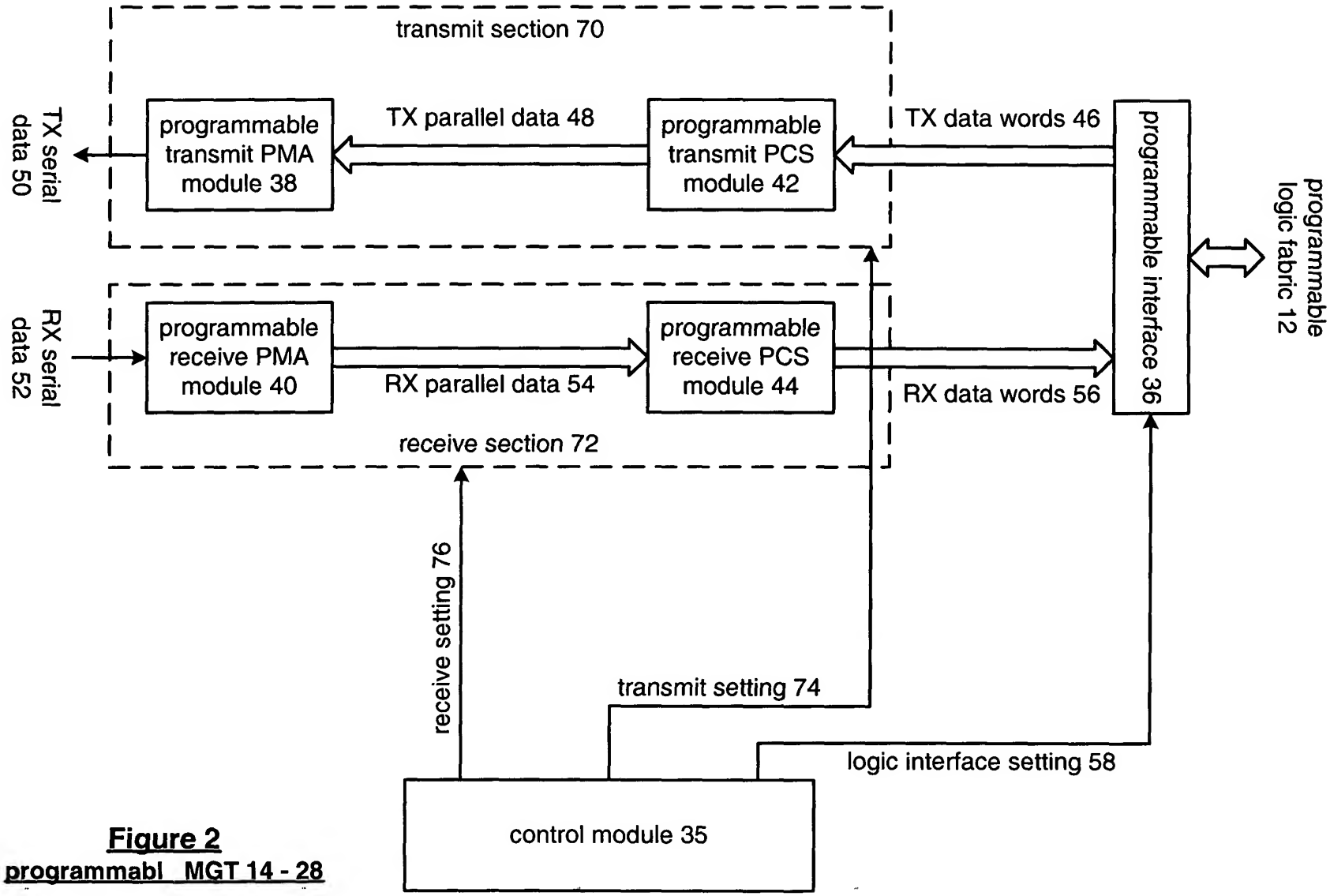


Figure 2
programmabl MGT 14 - 28

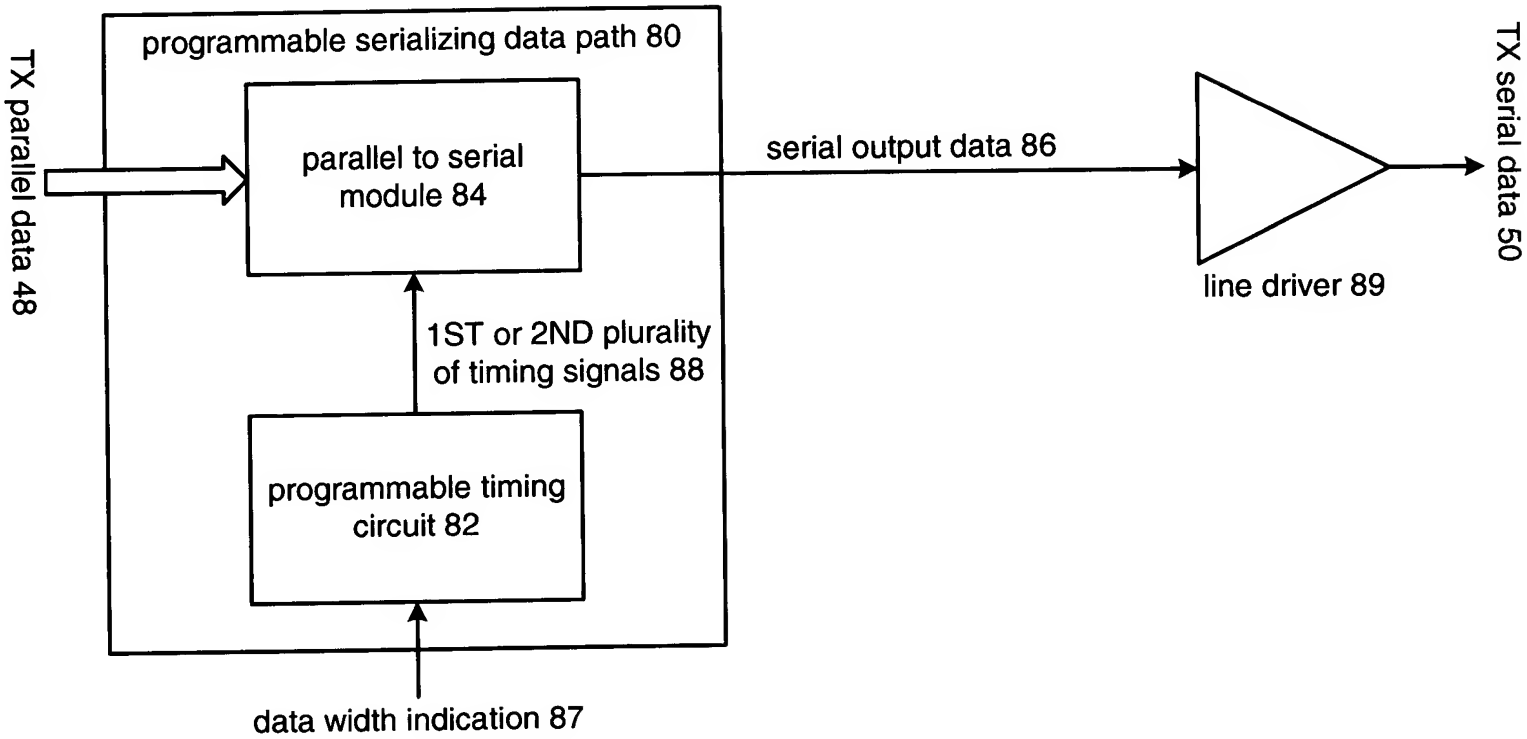


Figure 3
programmable transmit PMA module 38

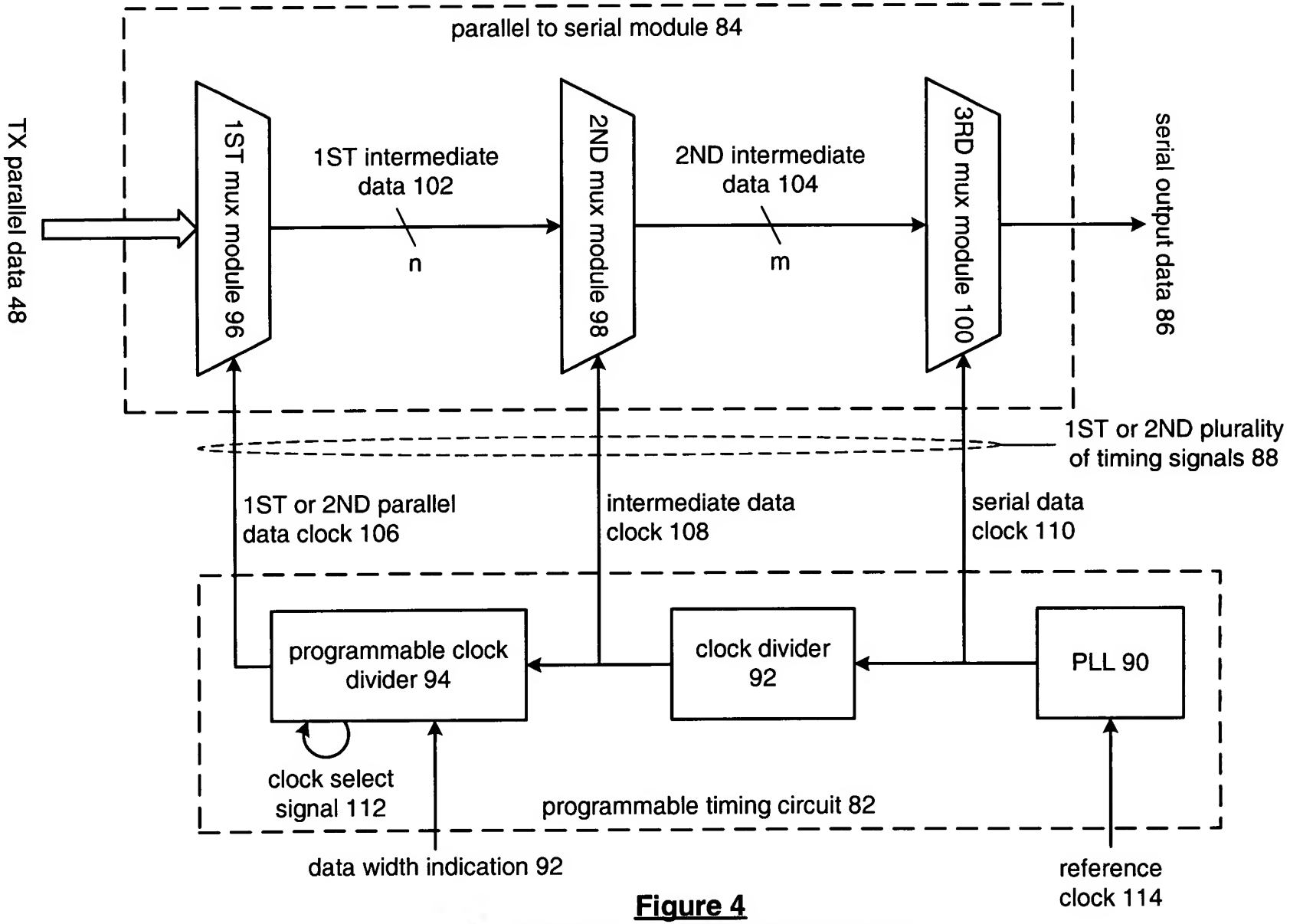


Figure 4

programmabl serializing data path 80

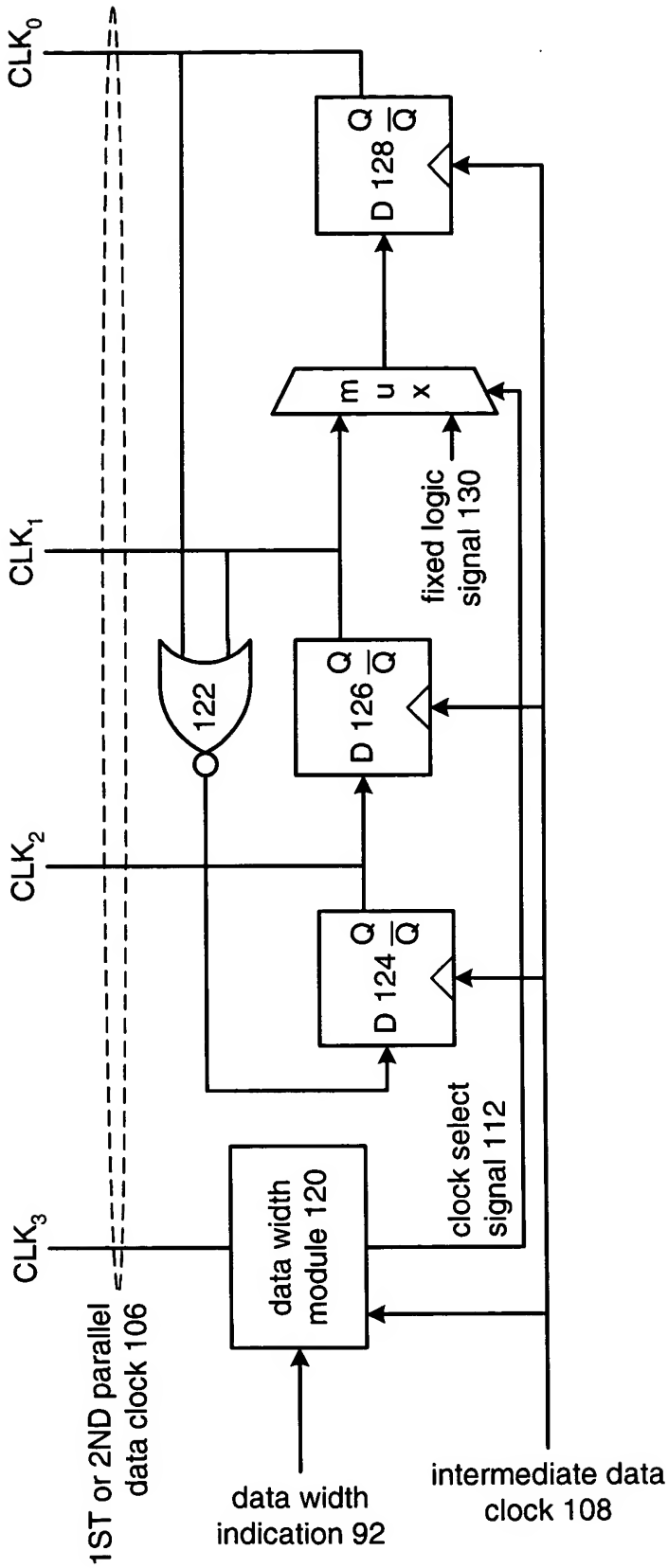


Figure 5
programmable clock divider 94

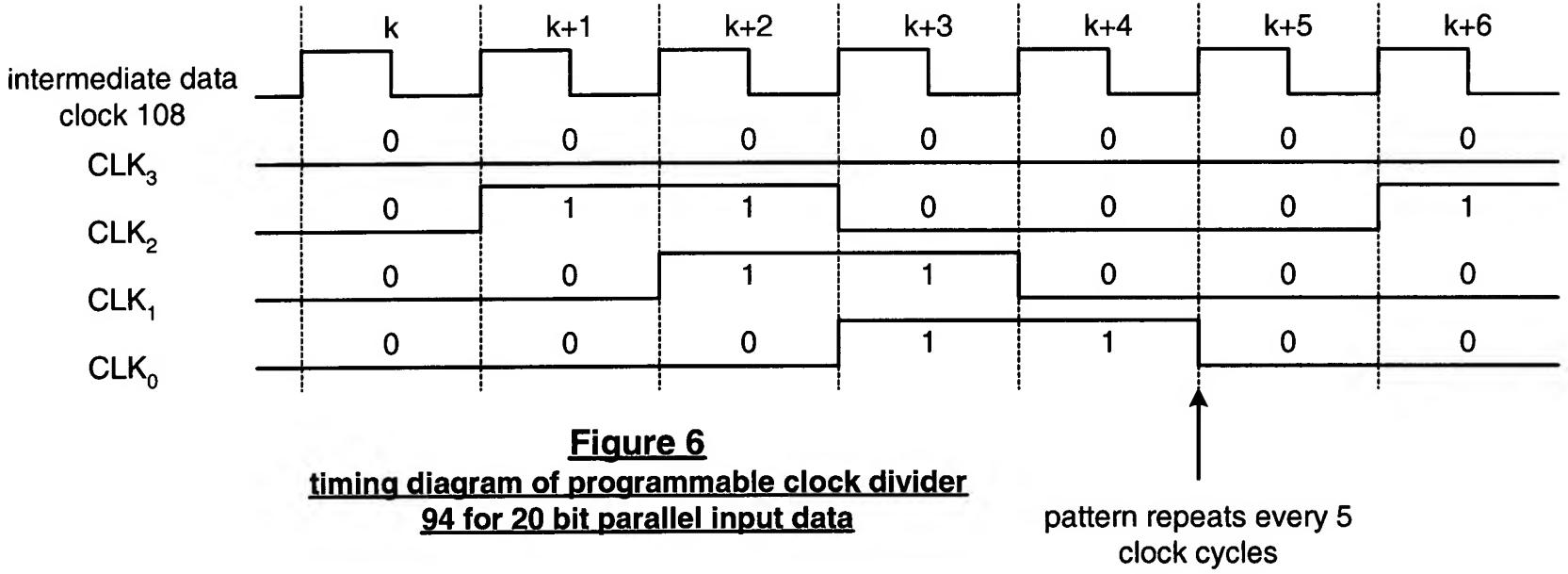


Figure 6

timing diagram of programmable clock divider 94 for 20 bit parallel input data

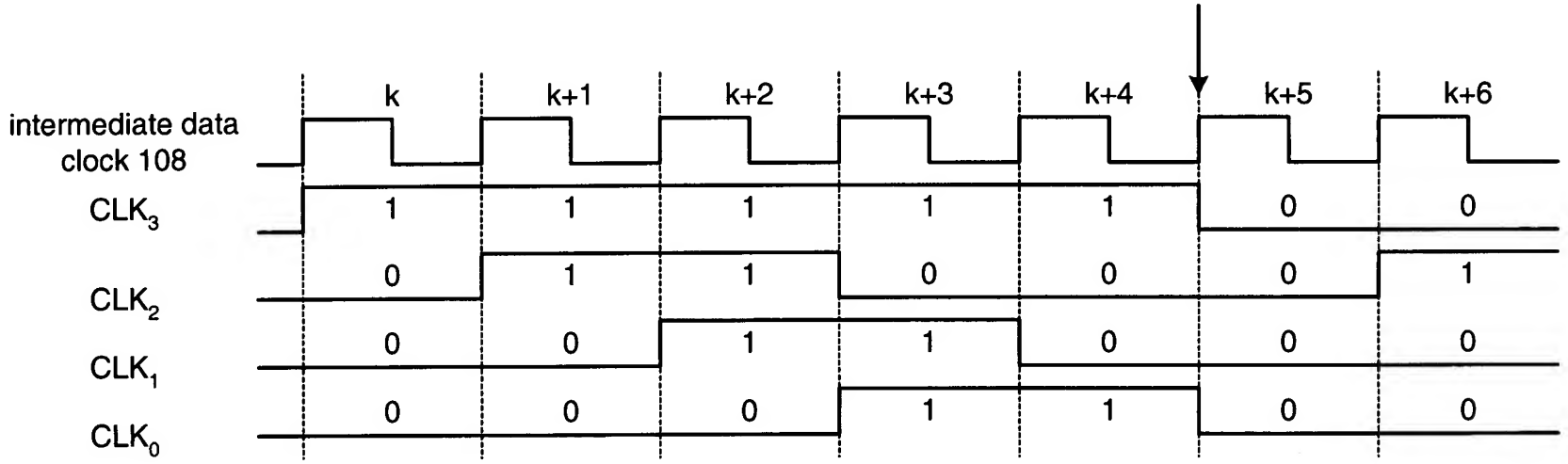


Figure 7

timing diagram of programmabl clock divid r 94 for 40 bit parallel input data

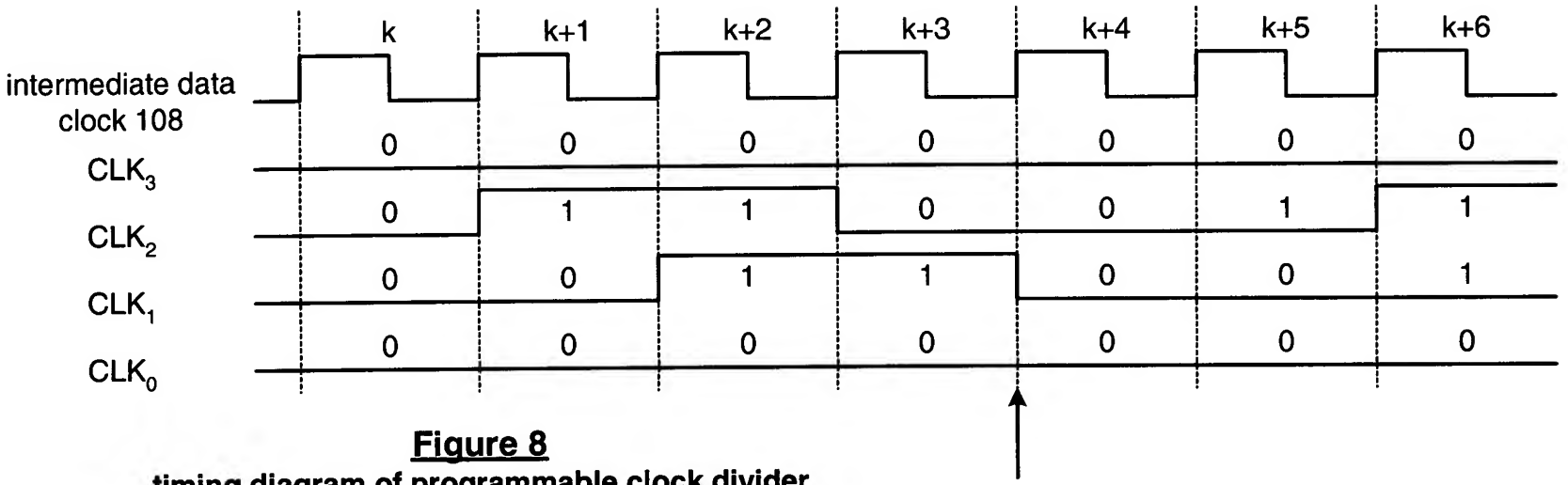


Figure 8

timing diagram of programmable clock divider 94 for 16 bit parallel input data

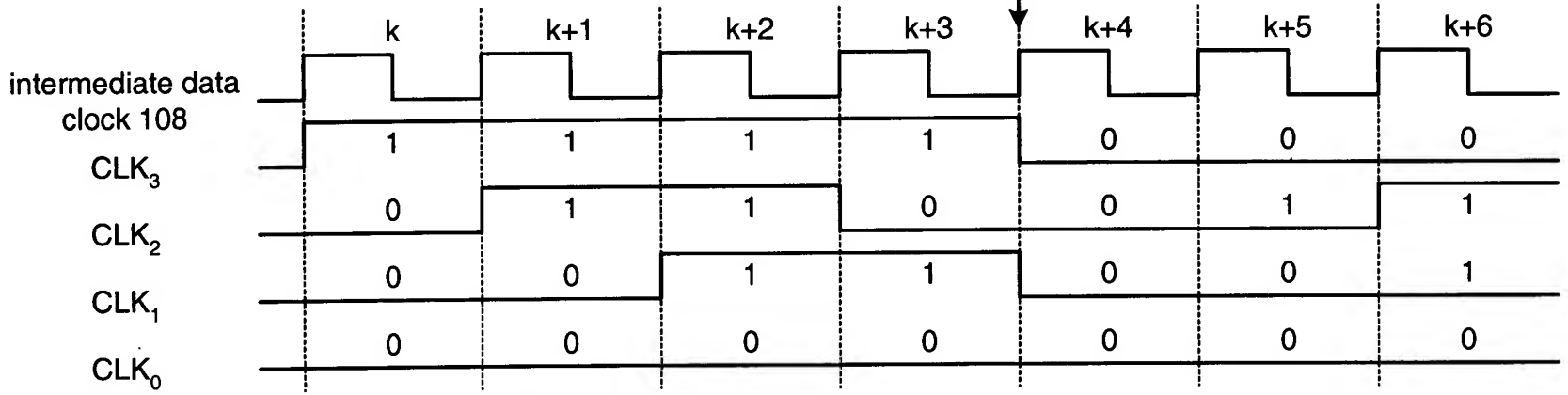


Figure 9

timing diagram of programmable clock divider 94 for 32 bit parallel input data

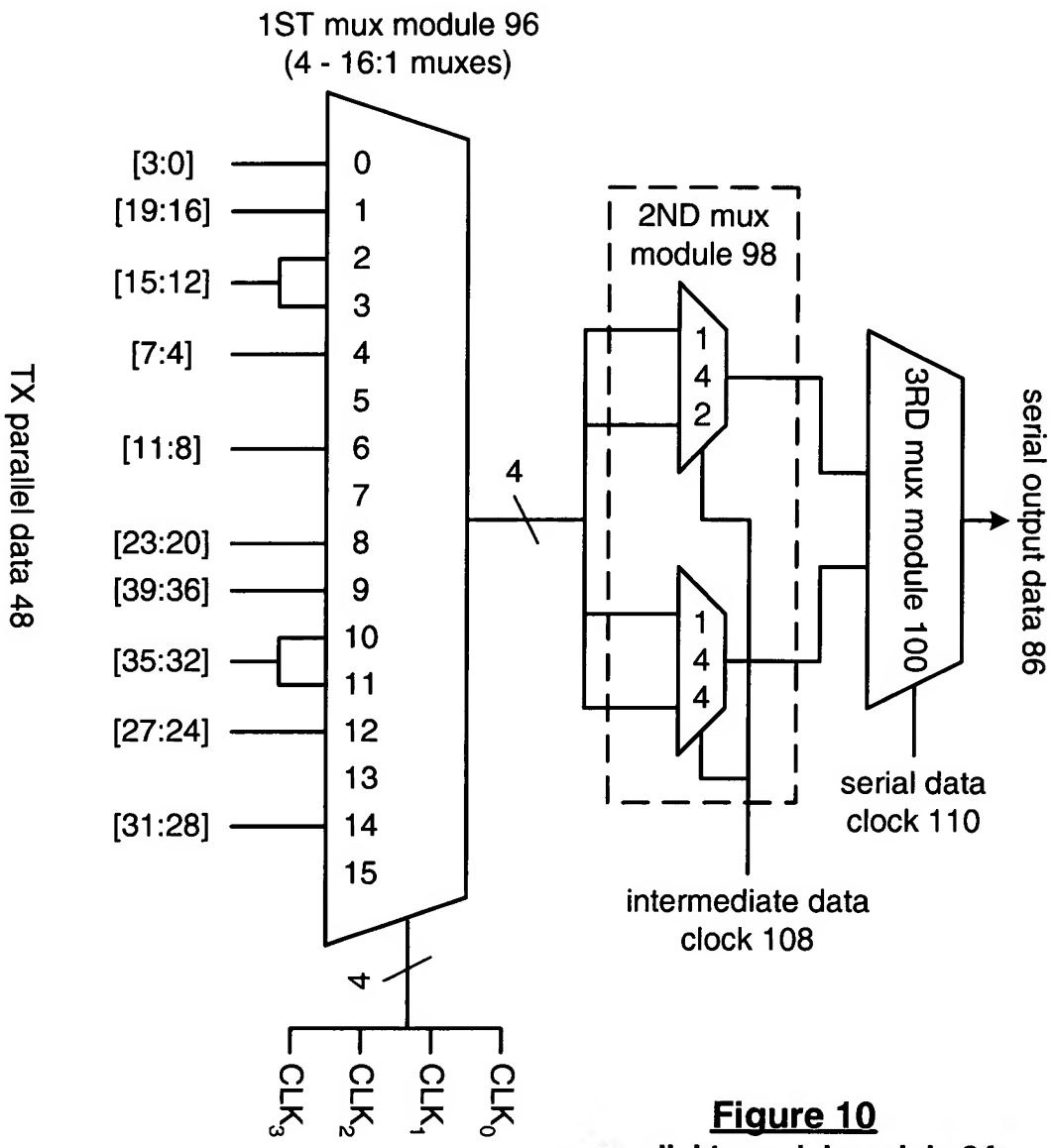
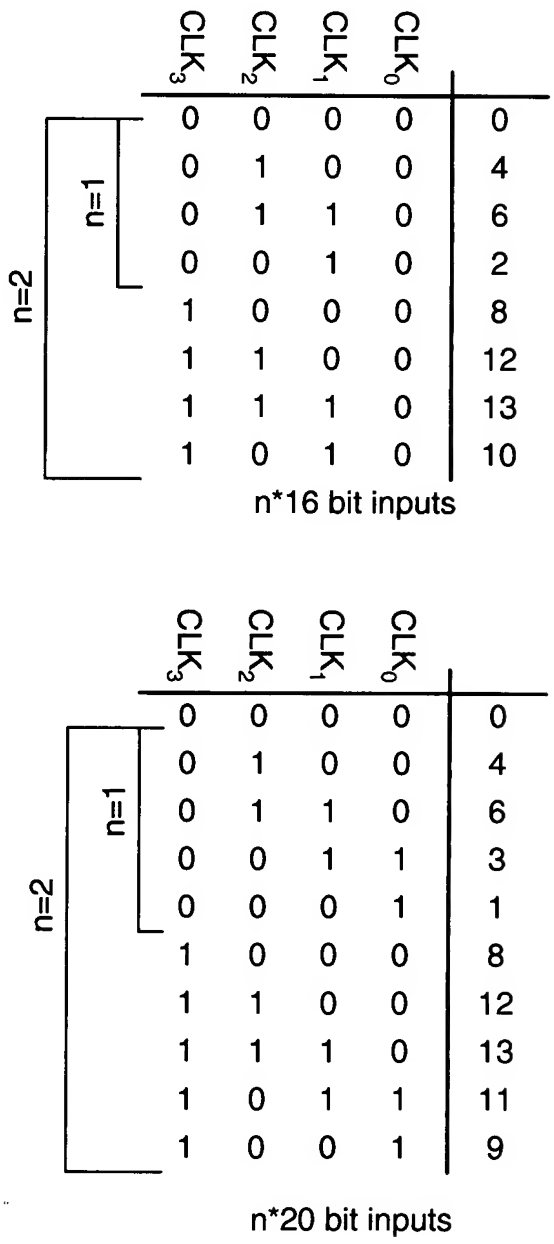


Figure 10
parall l to s rial modul 84



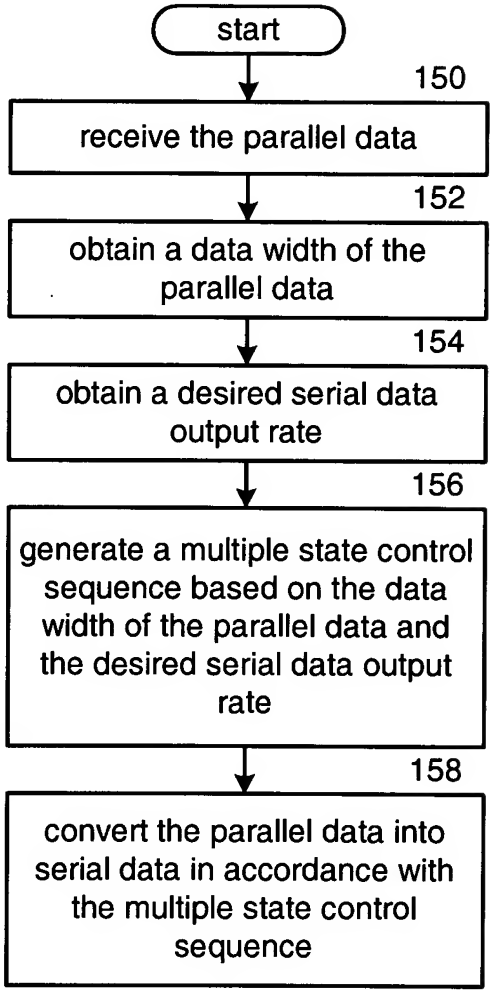

start
150
receive the parallel data
152
obtain a data width of the parallel data
154
obtain a desired serial data output rate
156
generate a multiple state control sequence based on the data width of the parallel data and the desired serial data output rate
158
convert the parallel data into serial data in accordance with the multiple state control sequence

Figure 11